Claims 17 and 19 have been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejections.

Applicants respectfully traverse the Examiner's objection to the term "core" in claims 6 and 36-39, as being given a meaning repugnant to the usual meaning of the term. The Examiner states that the accepted meaning of the term "core" is "one of the types memory built into computers before RAM or main memory." Applicants submit herewith a copy of pages 187 and 188 of the Glossary of DSP Processor Fundamentals, 1994, which defines the term "core" as being:

> Refers to the central execution units of a processor, **excluding such things as memory** and peripherals. In many cases, DSP processor manufacturers use a common core with different combinations of memory and peripherals to create a family of processors with the same architecture. Some vendors provide DSP cores that their customers can use to create their own customized application-specific ICs.

Accordingly, Applicants' use of the term "core" is consistent with the usual meaning of the term in the processor art. The Examiner's definition of the term is supposition not supported by fact. Accordingly, the above objection is overcome.

Claims 6-7, 9, 10-15, 17 and 36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al. (4,964,035) in view of Asano et al., (5,237,686). Applicants respectfully traverse this rejection.

Independent Claim 6 requires and positively recites, "a first processor for performing scalar processing, said first processor comprising a core, **a program memory and a local memory**", "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "a

memory circuit **for coupling said local memory of said first processor to said local memory of said second processor**".

Independent Claim 36 requires and positive recites, "a first processor comprising a core, **a program memory and a local memory**", "a second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-

DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Applicants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 36, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing. Accordingly, the 35 U.S.C. 103 rejection of Claims 6 and 36 of a combination of Aoyama and Asano is overcome.

Claims 7, 9, 10-15 and 17 stand allowable as depending from allowable claims and include further limitation not taught or suggested by the references of record.

Claim 7 further defines the apparatus of Claim 6, wherein said second processor is the main processor of said apparatus. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Moreover, since Asano fails to teach or suggest the use of a "main" processor with processors DMM1-DMMk, it fails to overcome the previously identified deficiency of the Aoyama reference.

Claim 9 further defines the apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP". The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 7.

Claim 10 further defines the apparatus of Claim 6, wherein said program memory of said first processor is ROM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 11 further defines the apparatus of Claim 6, wherein said local memory of said first processor is RAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 12 further defines the apparatus of Claim 6, wherein said program memory of said second processor is ROM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 13 further defines the apparatus of Claim 6, wherein said local memory of said second processor is RAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 14 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 15 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second

processor is a DPRAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 17 further defines the apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claims 8 and 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Mano. Applicants respectfully traverse this rejection.

Claim 8 further defines the apparatus of Claim 7, wherein said first processor is a microprocessor. Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.

The Examiner admits that Aoyama does not show the scalar processor as a microprocessor (Office Action dated May 15, 2001, page 7, line 18). Asano fails to teach or suggest a "scalar processor" or "a scalar processor that is a microprocessor". While Applicants agree with the Examiner that Mano discusses providing a processor into a microprocessor, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references as applied to Claims 6 and 7. Accordingly, the 35 U.S.C. 103 rejection is overcome.

Claims 19, 34-35 and 37-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Applicants' admitted prior art. Applicants respectfully traverse this rejection.

Claim 19 further defines the apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers; transfer corresponding to the transfer operations between a register in said protocol processor and memory; and monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6. Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 19 is overcome.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art

with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 34 is overcome.

Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of a n application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 35 is overcome.

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core**, a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said

core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, **a program memory and a local memory**, said protocol processor being suited to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4 & page 11, lines 14-17). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7 & page 11, lines 17-12).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-

DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Applicants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Applicants further point out that the Examiner admits that Aoyama and Asano "do not show the use of the first processor being a protocol processor", (Office Action dated May 15, 2001, page 12, lines 7-8). The Examiner relies upon Applicants' specification page 1, line 6 - page 2, line 11 for teaching that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art.

Applicants respectfully disagree with the Examiner interpretation of page 1, line 6 - page 2, line 11 of the instant specification. While "protocol processing" may itself be known in the art, there is no teaching or suggestion in Applicants' prior art that it could be combined with the teaching of Aoyama and Asano to obviate the present invention. Applicants further submit that the teaching of page 1, line 6 - page 2, line 11 of the instant specification does not overcome the previously identified deficiencies of the Aoyama and Asano references. Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 37 & 39, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, in combination with the teaching of page 1, line 6 - page 2, line 11 of the instant specification. Accordingly, the 35 U.S.C. 103 rejection of Claims 37-39 over a combination of Aoyama, Asano and Applicant's prior art is overcome.

Claims 19, 34-35 and 37-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Finch. Applicants respectfully traverse this rejection.

Claim 19 further defines the apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers; transfer corresponding to the transfer operations between a register in said protocol processor and memory; and monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6. Even if, arguendo, Finch discloses "a protocol processor performing protocol processing", Applicants' response is "so what"? Finch does not overcome the previously discussed deficiencies of Aoyama and Asano and there is no teaching or suggestion in Finch suggesting that it could be combined with the teachings of Aoyama and Asano in the manner suggested by the Examiner. Accordingly, the 35 U.S.C. 103 rejection of Claim 19 is overcome.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Even if, arguendo, Finch discloses "a protocol processor performing protocol processing", Applicants' response is "so what"? Finch does not overcome the previously discussed deficiencies of Aoyama and Asano and there is no teaching or suggestion in Finch suggesting that it could be combined with the teachings of Aoyama and Asano in the manner suggested by the Examiner. Accordingly, the 35 U.S.C. 103 rejection of Claim 34 is overcome.

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core**, a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory

coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, **a program memory and a local memory**, said protocol processor being suited to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4 & page 11, lines 14-17 & page 14, lines 13-16). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7 & page 11, lines 17-12 & page 14, lines 16-20).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it

would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Applicants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Applicants further point out that the Examiner admits that Aoyama and Asano "do not show the use of the first processor being a protocol processor", (Office Action dated May 15, 2001, page 12, lines 7-8 & page 15, lines 6 & 7). The Examiner relies upon Finch (col. 8, line 42 and et seq.) for teaching that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art.

Applicants respectfully disagree with the Examiner interpretation of page 1, line 6 - page 2, line 11 of the instant specification. While "protocol processing" may itself be known in the art, there is no teaching or suggestion in Applicants' prior art that it could be combined with the teaching of Aoyama and Asano to obviate the present invention. Applicants fail to understand how adding the teaching of page 1, line 6 - page 2, line 11 of the instant specification overcomes the previously identified deficiencies of the Aoyama and Asano references.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as

required by Claim 37 & 39, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, in combination with the teaching of page 1, line 6 - page 2, line 11 of the instant specification. Accordingly, the 35 U.S.C. 103 rejection of Claims 37-39 over a combination of Aoyama, Asano and Applicant's prior art is overcome.

Claims 6-15, 17, 19 and 34-39 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

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